WHAT IS CLAIMED IS:

1. A parasitic capacitance extracting device for a semiconductor integrated circuit, comprising:

a parasitic capacitance value information calculator configured to extract a dummy wiring pattern model from a wiring pattern library specifying wiring patterns of multilayer structure including said dummy wiring pattern model to replace said dummy wiring pattern model with a replacing insulator, thereby obtaining parasitic capacitance value information in which a value of a parasitic capacitance parasiting said replacing insulator is in correspondence with said dummy wiring pattern model, said replacing insulator having a dielectric constant higher than that of an interlayer insulation film isolating a wiring pattern of another layer from said dummy wiring pattern model; and

a parasitic capacitance extractor configured to receive layout pattern data specifying a semiconductor integrated circuit from which a parasitic capacitance is to be extracted and an extraction rule for extracting a dummy wiring pattern and to extract said dummy wiring pattern from said layout pattern data, thereby extracting a parasitic capacitance value corresponding to said dummy wiring pattern as extracted based on information related to said parasitic capacitance value information.

2. The parasitic capacitance extracting device according to claim 1, further comprising

a regression analyzer configured to perform regression analysis on said parasitic capacitance value information to obtain regression equation information in which model size information specifying a size related to said dummy wiring pattern model is in correspondence with said parasitic capacitance value, wherein

said parasitic capacitance extractor includes an extractor for obtaining size information related to said dummy wiring pattern based on said layout pattern data and said extraction rule, thereby extracting a parasitic capacitance value corresponding to said size information referring to said model size information of said regression equation information.

3. The parasitic capacitance extracting device according to claim 1, wherein

said parasitic capacitance extractor includes an extractor for obtaining said dummy wiring pattern based on said layout pattern data and said extraction rule and performing pattern matching between said dummy wiring pattern and said dummy wiring pattern model in said parasitic capacitance value information, thereby extracting a parasitic capacitance value based on the result of pattern matching.

4. The parasitic capacitance extracting device according to claim 1, wherein

said layout pattern data is inputted to said parasitic capacitance extractor as layout pattern data in which said dummy wiring pattern is already inserted.

5. The parasitic capacitance extracting device according to claim 1, further comprising

a dummy wiring pattern inserter configured to receive layout pattern data in which said dummy wiring pattern is not yet inserted and dummy wiring pattern insertion criteria information specifying insertion criteria of said dummy wiring pattern, thereby inserting said dummy wiring pattern in said layout pattern in which said dummy wiring pattern is not yet inserted based on said dummy wiring pattern insertion criteria information, wherein

said parasitic capacitance extractor receives said layout pattern data in which said dummy wiring pattern is inserted by said dummy wiring pattern inserter.

6. A parasitic capacitance extracting method for a semiconductor integrated circuit, comprising the steps of:

(a) receiving layout pattern data specifying a layout structure of a semiconductor integrated circuit from which a parasitic capacitance is to be extracted, thereby extracting said dummy wiring pattern from said layout pattern data, said layout pattern data including a wiring pattern of multilayer structure and a dummy wiring pattern;

(b) replacing said dummy wiring pattern with a replacing insulator, said replacing insulator having a dielectric constant higher than that of an interlayer insulation film isolating a wiring pattern of another layer from said dummy wiring pattern; and

(c) extracting a value of a parasitic capacitance parasiting said replacing insulator based on a circuit specified by said layout pattern data after replacement with said replacing insulator.